

IN THE CLAIMS:

We claim:

1 1. A memory system comprising a plurality of T-RAM cells arranged in an array,
2 wherein each of the plurality of T-RAM cells includes a thyristor region beneath at least a
3 portion of a transfer gate region.

1 2. The memory system according to Claim 1, wherein the thyristor region
2 includes a buried vertical thyristor and the transfer gate region includes a horizontally
3 stacked pseudo-TFT transfer gate.

1 3. The memory system according to Claim 1, wherein each of the plurality of T-
2 RAM cells has a size of less than or equal to $8F^2$.

1 4. The memory system according to Claim 1, wherein the plurality of T-RAM
2 cells are fabricated on a semiconductor SOI or bulk wafer.

1 5. The memory system according to Claim 1, wherein a base of the thyristor
2 region is surrounded by a vertical surrounded gate.

1 6. The memory system according to Claim 5, wherein the vertical surrounded
2 gate contacts a wordline.

1 7. The memory system according to Claim 1, wherein the thyristor region and
2 the transfer gate region are connected by a lateral epitaxial grown n^+ region.

1 8. The memory system according to Claim 2, wherein a bitline contacts a
2 junction of the stacked pseudo-TFT transfer gate.

1 9. The memory system according to Claim 2, wherein the stacked pseudo-TFT
2 transfer gate contacts a wordline.

1 10. The memory system according to Claim 1, wherein each of the plurality of T-
2 RAM cells includes structure for the traversal of at least two wordlines there through.

1 11. The memory system according to Claim 2, wherein a vertical surrounded gate
2 is aligned with a base region of the buried vertical thyristor.

1 12. A T-RAM array comprising:
2 a plurality of T-RAM cells, wherein each of the plurality of T-RAM cells includes a
3 thyristor region beneath at least a portion of a transfer gate region.

1 13. The array according to Claim 12, wherein the thyristor region includes a
2 buried vertical thyristor and the transfer gate region includes a horizontally stacked pseudo-
3 TFT transfer gate.

1 14. The array according to Claim 12, wherein each of the plurality of T-RAM
2 cells has a size of less than or equal to $8F^2$.

1 15. The array according to Claim 12, wherein the plurality of T-RAM cells are
2 fabricated on a semiconductor SOI or bulk wafer.

1 16. The array according to Claim 12, wherein a base of the thyristor region is
2 surrounded by a surrounded gate.

1 17. The array according to Claim 12, wherein each of the plurality of T-RAM
2 cells includes structure for the traversal of at least two wordlines there through.

1 18. A method for fabricating a T-RAM array having a plurality of T-RAM cells,
2 the method comprising the steps of:
3 providing a semiconductor wafer;
4 fabricating a thyristor region having a thyristor for each of the plurality of T-RAM
5 cells over the semiconductor wafer; and

1 fabricating a surrounded gate for each of the plurality of T-RAM cells, wherein the
2 surrounded gate is aligned with a base region of the thyristor;

3 fabricating a transfer gate region having a transfer gate for each of the plurality of T-
4 RAM cells over at least a portion of the thyristor region.

1 19. The method according to Claim 18, wherein each of the plurality of T-RAM
2 cells has a size of less than or equal to $8F^2$.

1 20. The method according to Claim 18, wherein the semiconductor wafer is a
2 semiconductor SOI or bulk wafer.

1 21. The method according to Claim 18, wherein the thyristor is a vertical thyristor
2 and the transfer gate is a pseudo-TFT transfer gate.

1 22. The method according to Claim 18, further comprising the step of fabricating
2 first and second wordlines, wherein the first wordline contacts the surrounded gate and the
3 second wordline is integral with the transfer gate.

1 23. The method according to Claim 18, further comprising the step of fabricating
2 a plurality of bitline contacts throughout the T-RAM array; and
3 fabricating a plurality of bitlines and a plurality of bitline contacts contacting a
4 respective one of the plurality of bitlines, wherein each of the plurality of bitline contacts
5 connects the respective one of the plurality of bitlines to a junction of the transfer gate.

1 24. The method according to Claim 18, further comprising the step of providing
2 three layers on the semiconductor wafer prior to the step of fabricating the thyristor region,
3 wherein a first layer is provided on top of a buried oxide layer and is a p-type layer and a
4 second layer is provided on top of the first layer, said second layer is a nitride-oxide layer
5 having a nitride layer below an oxide layer.

1 25. The method according to Claim 24, wherein the step of fabricating the
2 thyristor region having the thyristor for each of the plurality of T-RAM cells over the
3 semiconductor wafer includes the steps of:
4 providing a mask over the semiconductor wafer;
5 etching the oxide layer of the second layer to form etched regions over the nitride
6 layer;
7 depositing polysilicon within the etched regions;
8 etching the polysilicon to form a pair of spacer gates for each of the plurality of T-
9 RAM cells;
10 etching the nitride layer of the second layer to the surface of the first layer to shape
11 the thyristor region; and
12 growing an n-p-n layer within the thyristor region to form the thyristor.

1 26. The method according to Claim 25, wherein the step of growing the n-p-n
2 layer includes the steps of:
3 fabricating a first n-type layer over the first layer using a first n-type doping implant;
4 fabricating an p-type layer over the first n-type layer using a p-type doping implant;
5 and
6 fabricating a second n-type layer over the p-type layer by using a second n-type
7 doping implant.

1 27. The method according to Claim 26, wherein the step of fabricating the first n-
2 type layer includes the step of using n-type doping with a dosage of between $2E13/cm^2$ and
3 $8E14/cm^2$; wherein the step of fabricating the p-type layer includes the step using a p-type
4 doping with a dosage of between $4E13/cm^2$ and $1E14/cm^2$; and wherein the step of
5 fabricating the second n-type layer includes the step of using an n-type doping with a dosage
6 of between $8E14/cm^2$ and $3E15/cm^2$.

1 28. The method according to Claim 18, wherein the step of fabricating the
2 transfer gate region having the transfer gate for each of the plurality of T-RAM cells over at
3 least a portion of the thyristor region includes the steps of:

- 1 fabricating an epi layer over the thyristor region;
- 2 providing a dielectric film over the epi layer;
- 3 depositing an insulating film over the dielectric film;
- 4 forming two gates within the insulating film; and
- 5 implanting an n⁺ dopant within the epi layer to form source and drain regions for the
- 6 transfer gate.



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